AMPAK Technology Inc.

正基科技股份有限公司

SPECIFICATION

PRODUCT NAME：AP72xxx Series

REVISION：04

DATE：August 13, 2024

Customer APPROVED	
Company	
Representative Signature	

PREPARED	REVIEW				APPROVED	DCC ISSUE
	PM	QA	ET			
			PE			
			ME			
			APPROVED			

正基科技股份有限公司

AP72xxx_Series

Data Sheet

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Taiwan

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Revision

Revision	Date	Description	Revised By
0.0	2024/01/17	- Initial Released	Ander Lee
0.1	2024/05/23	- Series Model Released	Ander Lee
0.2	2024/06/18	- Add series model part number - Update SIP module URL	Ander Lee
0.3	2024/08/02	- Add Carrier board information - Add Software introduction	Ander Lee
0.4	2024/08/13	- Update Block Diagram - Add series model name and support SIP list - Add Carrier board Video Display Interface	Ander Lee
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Contents

1. Introduction

1.1 Overview

The Ampak Smart Audio SoM (System on Module) platform is an advanced module specially designed and optimized for mid and high-end sound technology, feature-rich IP phones and terminals that require powerful processing and 3D graphics capabilities. The SoM supports a sophisticated GUI and multi-channel high-quality HD voice. This smart speaker solution is Artificial Intelligence (AI) Engine can be done on GPU and/or CPU, dedicated specifically for low-power, high-performance smart audio applications.

The SoM AP72XXX_SERIES is an advanced application processor designed for voice control and smart audio speaker / smart home applications. It integrates a powerful subsystem with Wi-Fi 4 & 6E (2.4/5/6GHz) **/** Bluetooth 5.2 & 5.3 and advanced multi-format audio DSP is complete audio front end addressing all audio in/out functionality expected from high-end VoIP terminals, providing two high-quality audio DACs and ADCs. The audio DSP has three differential input amplifiers and two differential output amplifiers which can support stereo and mono speakers, headsets, and/or line outputs. It supports digital microphone, hardware-controlled mute, and three individual analog mute inputs that function independently, capable of muting each of the three differential input amplifiers.

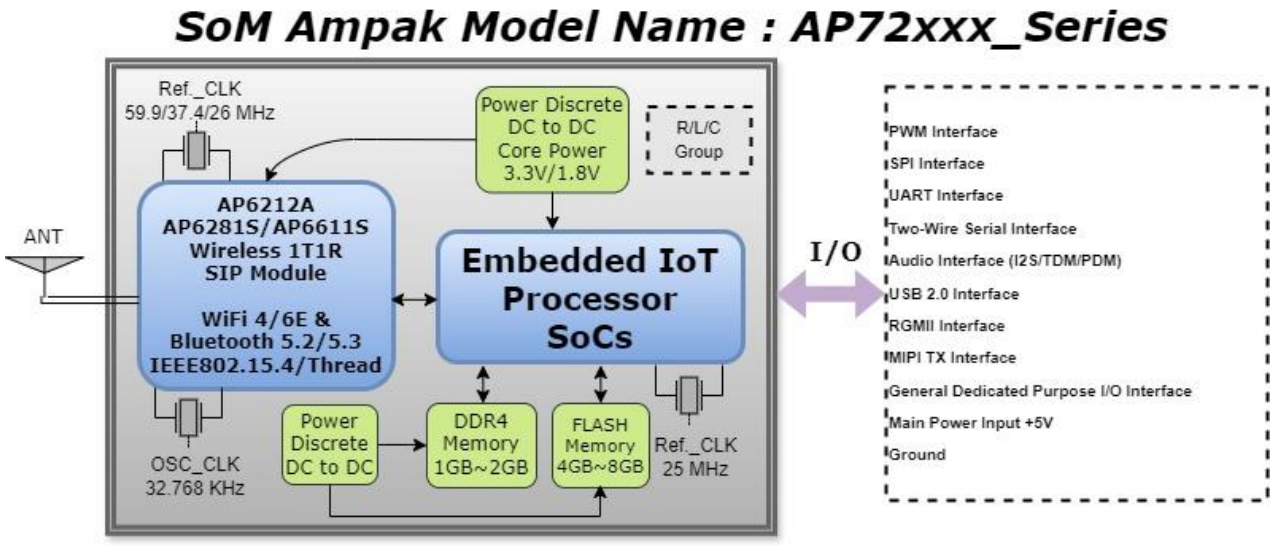


Figure 1-1 Block diagram

1.2 Product Features

- Wireless technology supports multi-mode communication protocols and is compatible with Ampak's 12x12mm pin to pin series products.
- Lead Free design which is compliant with ROHS requirements.
- CPU: Quad-core Arm® Cortex®-A55 up to 1.9GHz
- GPU
  - Imagination™ BXE-2-32 / Dual core (2 pixels per clock)
  - Clock frequency up to 800 MHz
  - Supports OpenGL® ES™ 3.2, OpenCL™ 3.0, EGL™ 1.5, Vulkan® 1.3, Android™ NN API through IMGDNN AP
- Security:
  - On-chip 32Kbit anti-fuse OTP
  - True random number generator
  - DRM engine supports
  - AES, DES, 3DES, SHA1/SHA2/MD5, RSA, ECC
- Audio
  - TDM//PDM and DVFA audio
  - 8 to 96/192 kHz and slot size 8/16/24/32 bit
- Memory Interfaces
    - DRAM 32-bit DDR4- 2666 up to 8 Gb memory space
    - 4Gb NAND 8 bit Parallel SLC (64 bit ECC per 2KB of data)
- Peripherals
  - One USB 3.0 Host and One USB 2.0 On-The-Go (OTG) interface
  - Four TWSI 2-wire buses (I2C compatible) and Two high speed UART interfaces
  - Two SPI controllers and Up to four slave devices supported on each interface
  - 72-bit pin-shared GPIOs
  - Rectangular Keyboard matrix controller up to 80 keys (8x10)
  - 4 PWMs and On-chip temperature sensor
- Video/Display Interfaces
  - MIPI Display Serial Interface (DSI) up to 1080p60 screen resolution
  - RGB Digital Parallel Interface (DPI) / CPU-type Display Bus Interface (DBI) , RGB 16bpp (565), 18bpp (666) and 24bpp (888) output formats / Up to 1080p30 screen resolution and refresh rate
- Ethernet
  - 802.3 (G)MAC supports RGMII and RMII
  - 802.1 p/q tagging (VLAN) in hardware
  - IEEE 1588 Precision Time Protocol (PTP) with PPS output signal
- IEEE 802.11 Key Features
  - TX and RX low-density parity check (LDPC) support for improved range and power efficiency.
  - Dual-stream spatial multiplexing up to 1200 Mbps data rate.
  - 20/40/80 MHz channels for 5GHz and 6GHz radio, and 20MHz channels for 2.4GHz radio.
  - Client MU-MIMO
- Bluetooth Key Features
  - Complies with Bluetooth Core Specification Version 5.3 with provisions for

supporting future specifications. With Bluetooth Class 1 or Class2 transmitter operation.

- Supports extended synchronous connections (eSCO), for enhanced voice quality by allowing for retransmission of dropped packets.
- Adaptive frequency hopping (AFH) for reducing radio frequency interference. A simplified block diagram of the module is depicted in the figure above.
- BT Core Specification Version 5.3, including the following support:
  - Low energy (LE) isochronous channels
  - LE power controls
  - LE enhanced connection updates
  - LE channel classification
  - LE audio

- IEEE 802.15.4/Thread Key Feature
  - Support IEEE 802.15.4/Thread that can act as Border Router.

- Package
  - 69.6x50x5.5mm SO-DIMM 260-pin

2. General Specification

2.1 General Specification

Model Name	AP72XXX_SERIES
Product Description	Smart Audio & Embedded IoT System on Module Support Wi-Fi 6E / Bluetooth 5.3 / IEEE 802.15.4 / Thread functionality
Dimension	SO-DIMM 260-pin L x W x H : 69.6(±0.15) x 50(±0.15) mm x 5.50(±0.2)mm
Operating temperature	0°C to 65°C
Storage temperature	-40°C to 85°C
Humidity	Operating Humidity 10% to 95% Non-Condensing Storage Humidity 5% to 95% Non-Condensing

2.2 Recommended Operating Rating

	Min.	Typ.	Max.	Unit
Operating Temperature	-10	25	65	deg.C
VDD	4.5	5	5.5	V

2.3 Product current consumption

Item	Typ.
work mode: CPU load 80%, TX or RX throughput 20Mbps,	TBD
idle mode: CPU load 0%, keep connection to AP but no wifi stream,	TBD
EUP mode: the lowest power ,can wake up by Wifi and BT.	TBD

3. Order Information

Model Name	Part Number	Common Features	Wireless Model	DDR Size	Flash Size	IEEE802.15.4/ Thread
AP72611	99P-W02-0656R	✧ Embedded IoT SOM ✧ Wi-Fi 6E Dual Band ✧ Bluetooth 5.3 ✧ 1T1R	AP6611S	2GB	8GB	Not Support
AP72611_1D4M	99P-W02-0666R			1GB	4GB	Not Support
AP72281	99P-W02-0667R		AP6281S	2GB	8GB	Support
AP72281_1D4M	99P-W02-0668R			1GB	4GB	Support
AP72212_1D4M	99P-W02-0672R	✧ Embedded IoT SOM ✧ Wi-Fi 4 ✧ Bluetooth 5.2, integrated Class 1.5 PA ✧ 1T1R	AP6212A	1GB	4GB	Not Support

4. Wireless Specification

4.1 AP6281S Wi-Fi6E/Bluetooth5.3/IEEE 802.15.4/Thread

- Please refer to the following specification sheet and refer to the detailed data sheet of AP6281S.
- URL:
  https://www.ampak.com.tw/product/WiFi-Bluetooth/stamp-type-1T1R/AP6281S
- For more information about our products please contact AMPAK sales.

Model Name	AP6281S
Product Description	1T1R 802.11 a/b/g/n/ac/ax Wi-Fi 6E + BT 5.3+ IEEE 802.15.4/Thread Module
Dimension	L x W : 12 x 12 (typical) mm ， H : 1.95 (Maximum) mm
WiFi Interface	Support SDIO V3.0/ 2.0
BT Interface	UART / PCM
Operating temperature	-30°C to 85°C
Storage temperature	-40°C to 125°C
Humidity	Operating Humidity 10% to 95% Non-Condensing Storage Humidity 5% to 95% Non-Condensing

4.2 AP6611S Wi-Fi6E/Bluetooth5.3

- Please refer to the following specification sheet and refer to the detailed data sheet of AP6611S.
- URL:
  https://www.ampak.com.tw/product/WiFi-Bluetooth/stamp-type-1T1R/AP6611S
- For more information about our products please contact AMPAK sales.

Model Name	AP6611S
Product Description	1T1R 802.11 a/b/g/n/ac/ax Wi-Fi 6E + BT 5.3 Module
Dimension	L x W : 12 x 12 (typical) mm ， H : 1.67 (Maximum) mm
Module type package	Stamp type with metal lid
Wi-Fi Interface	Support SDIO V3.0/ 2.0
BT Interface	UART / PCM
Operating temperature	-30°C to 85°C
Storage temperature	-40°C to 125°C
Humidity	Operating Humidity 10% to 95% Non-Condensing Storage Humidity 5% to 95% Non-Condensing

4.3 AP6212A Wi-Fi4 / Bluetooth5.2

802.11b/g/n single-band radio
Bluetooth V5.2 with integrated Class 1.5 PA and Low Energy (BLE) support

✧ Please refer to the following specification sheet and refer to the detailed data sheet of AP6212A.

✧ URL:
https://www.ampak.com.tw/product/WiFi-Bluetooth/stamp-type-1T1R/AP6212

✧ For more information about our products please contact AMPAK sales.

Model Name	AP6212A
Product Description	Support Wi-Fi 4/Bluetooth5.2 functionalities
Dimension	L x W : 12 x 12 (typical)mm，H:1.7 (Maximum) mm
Wi-Fi Interface	SDIO V2.0
BT Interface	UART / PCM
Operating temperature [a,b]	-30°C to 85°C
Storage temperature	-40°C to 85°C
Humidity	Operating Humidity 10% to 95% Non-Condensing Storage Humidity 5% to 95% Non-Condensing

a. The operating temperature 65 to 85°C is feasible at conditional environment. Please examine the reliability on final product.

b. Functionality is guaranteed across this range of temperature. Optimal RF performance as specified in the data sheet.
However, is guaranteed only for –10°C to 55°C and 3.2V < VBAT <3.8V

5. Software Introduction

5.1 Astra Introduction

Astra™ is the new Synaptics' compute platform designed for the IoT market. It features a series of high-performance, AI-native, multi-modal SoCs optimized for consumer, enterprise, and industrial IoT workloads. These SoCs come equipped with hardware accelerators for edge inferencing, security, graphics, vision, and audio, and offer out-of-box functionality with Synaptics connectivity.

Astra (v1.0.0) GA Release is a unified software development kit supporting the SL-Series of MPUs.

The high-level components included in this SDK are described below:

- Upstream Linux Kernel and device tree.
- Low-level Linux device drivers (U-BOOT) for peripheral devices.
- Open source code for Multimedia and VOIP pipelines.
- Synaptics proprietary security approach.
- Related SDK Documents

All of these items can be found through Synaptics' and third parties open source Git repositories on GitHub.

5.2 Yocto SDK

The Yocto Project is an open-source collaboration project that provides templates, tools and methods for custom Linux-based systems for embedded and IoT products. By leveraging the power of the open-source development community, Synaptics hopes to provide its customers with a wider array of compatible software packages to build their products faster, with more features, while at the same time having the stability and support of a large open-source development project. Additionally, the SDK enables customers who already use a Yocto-based development environment to migrate to Synaptics class-leading silicon solutions for improved performance and additional functionality. The Yocto Project offers a vast number of software packages that provide many options.

5.3 License

Using the Astra Software Developer Kit and BSP requires complying with the ASTRA EMBEDDED SOFTWARE DEVELOPMENT KIT LICENSE AGREEMENT –.

https://synaptics-astra.github.io/doc/v/1.0.0/EULA.html

5.4 Synaptics Proprietary TAs

The following Trusted Applications (TAs) are Synaptics proprietary TAs which run in the OP-TEE Trusted Execution Environment. They are provided in binary format. Synaptics will migrate them into REE and open source the code to the public in a near future releases.

Package	Notes
MIPI-DSI	TA SL1620
Fastlogo	TA SL1680 / SL1640
SyNAP	TA SL1680 / SL1640 / SL1620
DHUB	TA SL1680 / SL1640
Vmeta	TA SL1680 / SL1640 / SL1620

5.5 Where to get the SDK from GitHub

5.5.1 Images and Toolchains

https://github.com/synaptics-astra/sdk/releases/

5.5.2 SDK

https://github.com/synaptics-astra/sdk/tree/v1.0.0

5.6 Documentation

Getting Started

https://synaptics-astra.github.io/doc/v/1.0.0/quickstart/index.html

Astra Yocto Linux Developer Guide

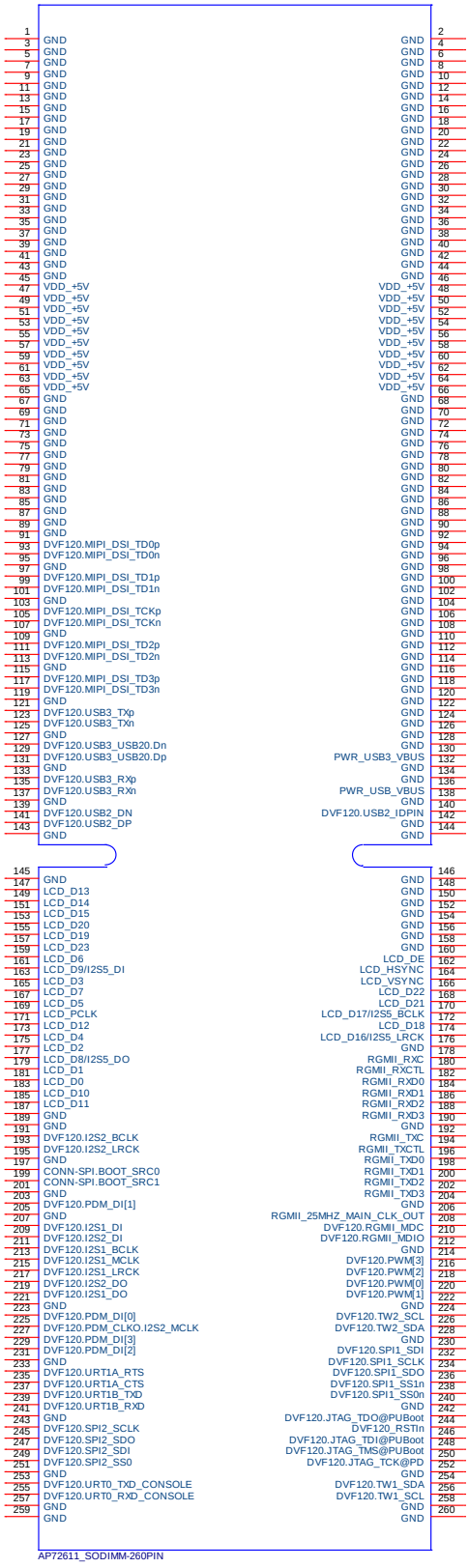
https://synaptics-astra.github.io/doc/v/1.0.0/yocto.html

Astra Yocto Linux User Guide

https://synaptics-astra.github.io/doc/v/1.0.0/linux/index.html

6. Pin Definition

6.1 Pin Outline Diagram



6.2 Pin Assignment

260-Pin SODIMM Front			
Pin #	**Pin Name**	**Pin Type**	**Description**
1	GND	Power	Ground
3	GND	Power	Ground
5	GND	Power	Ground
7	GND	Power	Ground
9	GND	Power	Ground
11	GND	Power	Ground
13	GND	Power	Ground
15	GND	Power	Ground
17	GND	Power	Ground
19	GND	Power	Ground
21	GND	Power	Ground
23	GND	Power	Ground
25	GND	Power	Ground
27	GND	Power	Ground
29	GND	Power	Ground
31	GND	Power	Ground
33	GND	Power	Ground
35	GND	Power	Ground
37	GND	Power	Ground
39	GND	Power	Ground
41	GND	Power	Ground
43	GND	Power	Ground
45	VDD_+5V	Power	Input Main Power DC +5V
47	VDD_+5V	Power	Input Main Power DC +5V
49	VDD_+5V	Power	Input Main Power DC +5V
51	VDD_+5V	Power	Input Main Power DC +5V
53	VDD_+5V	Power	Input Main Power DC +5V
55	VDD_+5V	Power	Input Main Power DC +5V
57	VDD_+5V	Power	Input Main Power DC +5V
59	VDD_+5V	Power	Input Main Power DC +5V
61	VDD_+5V	Power	Input Main Power DC +5V
63	VDD_+5V	Power	Input Main Power DC +5V

65	GND	Power	Ground
67	GND	Power	Ground
69	GND	Power	Ground
71	GND	Power	Ground
73	GND	Power	Ground
75	GND	Power	Ground
77	GND	Power	Ground
79	GND	Power	Ground
81	GND	Power	Ground
83	GND	Power	Ground
85	GND	Power	Ground
87	GND	Power	Ground
89	GND	Power	Ground
91	MIPI_DSI_D0p	CMOS, Output	MIPI TX Data lane 0 +ve line
93	MIPI_DSI_D0n	CMOS, Output	MIPI TX Data lane 0 -ve line
95	GND	Power	Ground
97	MIPI_DSI_D1p	CMOS, Output	MIPI TX Data lane 1 +ve line
99	MIPI_DSI_D1n	CMOS, Output	MIPI TX Data lane 1 -ve line
101	GND	Power	Ground
103	MIPI_DSI_CKp	CMOS, Output	MIPI TX Clock lane +ve line
105	MIPI_DSI_CKn	CMOS, Output	MIPI TX Clock lane -ve line
107	GND	Power	Ground
109	MIPI_DSI_D2p	CMOS, Output	MIPI TX Data lane 2 +ve line
111	MIPI_DSI_D2n	CMOS, Output	MIPI TX Data lane 2 -ve line
113	GND	Power	Ground
115	MIPI_DSI_D3p	CMOS, Output	MIPI TX Data lane 3 +ve line
117	MIPI_DSI_D3n	CMOS, Output	MIPI TX Data lane 3 -ve line
119	GND	Power	Ground
121	USB3_TXp	Analog, Input	USB 3.0 SS Transmit Port Data Positive
123	USB3_TXn	Analog, Input	USB 3.0 SS Transmit Port Data Negative
125	GND	Power	Ground
127	USB3_USB20.Dn	Analog, Input/Output	USB 3.0 Port Data Negative (USB20)
129	USB3_USB20.Dp	Analog, Input/Output	USB 3.0 Port Data Positive (USB20)
131	GND	Power	Ground
133	USB3_RXp	Analog, Input	USB 3.0 SS Receive Port Data Positive
135	USB3_RXn	Analog, Input	USB 3.0 SS Receive Port Data Negative
137	GND	Power	Ground

139	USB2_Dn	Analog, Input/Output	USB 2.0 Port Data Negative
141	USB2_Dp	Analog, Input/Output	USB 2.0 Port Data Positive
143	GND	Power	Ground
145	GND	Power	Ground
147	LCDD13	CMOS, Input/Output	LCDC (RGB) Interface Data 13
149	LCDD14	CMOS, Input/Output	LCDC (RGB) Interface Data 14
151	LCDD15	CMOS, Input/Output	LCDC (RGB) Interface Data 15
153	LCDD20	CMOS, Input/Output	LCDC (RGB) Interface Data 20
155	LCDD19	CMOS, Input/Output	LCDC (RGB) Interface Data 19
157	LCDD23	CMOS, Input/Output	LCDC (RGB) Interface Data 23
159	LCDD6	CMOS, Input/Output	LCDC (RGB) Interface Data 6
161	LCDD9 / I2S5_DI	CMOS, Input/Output	LCDC (RGB) Interface Data 9 / Audio Interface #5 Data in
163	LCDD3	CMOS, Input/Output	LCDC (RGB) Interface Data 3
165	LCDD7	CMOS, Input/Output	LCDC (RGB) Interface Data 7
167	LCDD5	CMOS, Input/Output	LCDC (RGB) Interface Data 5
169	LCD_PCLK	CMOS, Input/Output	LCDC (RGB) Interface Clock Output
171	LCDD12	CMOS, Input/Output	LCDC (RGB) Interface Data 12
173	LCDD4	CMOS, Input/Output	LCDC (RGB) Interface Data 4
175	LCDD2	CMOS, Input/Output	LCDC (RGB) Interface Data 2
177	LCDD8 / I2S5_DO	CMOS, Input/Output	LCDC (RGB) Interface Data 8 / Audio Interface #5 Data out
179	LCDD1	CMOS, Input/Output	LCDC (RGB) Interface Data 1
181	LCDD0	CMOS, Input/Output	LCDC (RGB) Interface Data 0
183	LCDD10	CMOS, Input/Output	LCDC (RGB) Interface Data 10

185	LCDD11	CMOS, Input/Output	LCDC (RGB) Interface Data 11
187	GND	Power	Ground
189	GND	Power	Ground
191	I2S2_BCLK	CMOS, Input/Output	Audio Interface #2 bit clock
193	I2S2_LRCK	CMOS, Input/Output	Audio Interface #2 WS or LR select
195	GND	Power	Ground
197	CONN-SPI.BOOT_SRC 0	CMOS, Input	External SPI Bootloader Control SRC0, Active LOW
199	CONN-SPI.BOOT_SRC 1	CMOS, Input	External SPI Bootloader Control SRC1, Active LOW
201	GND	Power	Ground
203	PDM_DI[1]	CMOS, Input	PDM Data in channel 1
205	GND	Power	Ground
207	I2S1_DI	CMOS, Input	Audio Interface #1 Data in
209	I2S2_DI	CMOS, Input	Audio Interface #2 Data in
211	I2S1_BCLK	CMOS, Input/Output	Audio Interface #1 bit clock
213	I2S1_MCLK	CMOS, Input/Output	Audio Interface #1 Master clock
215	I2S1_LRCK	CMOS, Input/Output	Audio Interface #1 WS or LR select
217	I2S2_DO	CMOS, Output	Audio Interface #2 Data out
219	I2S1_DO	CMOS, Output	Audio Interface #1 Data out
221	GND	Power	Ground
223	PDM_DI[0]	CMOS, Input	PDM Data in channel 0
225	PDM_CLKIO / I2S2_MCLK	CMOS, Output	PDM Clock out / Audio Interface #2 Master clock
227	PDM_DI[3]	CMOS, Input	PDM Data in channel 3
229	PDM_DI[2]	CMOS, Input	PDM Data in channel 2
231	GND	Power	Ground
233	UART1A_RTS	CMOS, Output	UART1 RTS location A
235	UART1A_CTS	CMOS, Input	UART1 CTS location A
237	UART1B_TX	CMOS, Output	UART1 TX location B
239	UART1B_RX	CMOS, Input	UART1 RX location B
241	GND	Power	Ground
243	SPI2_SCLK	CMOS, Output	SPI2 serial clock.
245	SPI2_SDO	CMOS, Input/Output	SPI2 serial data output

247	SPI2_SDI	CMOS, Input	SPI2 serial data input
249	SPI2_SS0n	CMOS, Output	SPI2 Module select 0 For first slave device with handler
251	GND	Power	Ground
253	UART0A_TX	CMOS, Output	UART0 TX location A/URT0_TXD_CONSOLE
255	UART0A_RX	CMOS, Input	UART0 RX location A/URT0_RXD_CONSOLE
257	GND	Power	Ground
259	GND	Power	Ground

260-Pin SODIMM Back			
Pin #	**Pin Name**	**Pin Type**	**Description**
2	GND	Power	Ground
4	GND	Power	Ground
6	GND	Power	Ground
8	GND	Power	Ground
10	GND	Power	Ground
12	GND	Power	Ground
14	GND	Power	Ground
16	GND	Power	Ground
18	GND	Power	Ground
20	GND	Power	Ground
22	GND	Power	Ground
24	GND	Power	Ground
26	GND	Power	Ground
28	GND	Power	Ground
30	GND	Power	Ground
32	GND	Power	Ground
34	GND	Power	Ground
36	GND	Power	Ground
38	GND	Power	Ground
40	GND	Power	Ground
42	GND	Power	Ground
44	GND	Power	Ground
46	VDD_+5V	Power	Input Main Power DC +5V
48	VDD_+5V	Power	Input Main Power DC +5V
50	VDD_+5V	Power	Input Main Power DC +5V

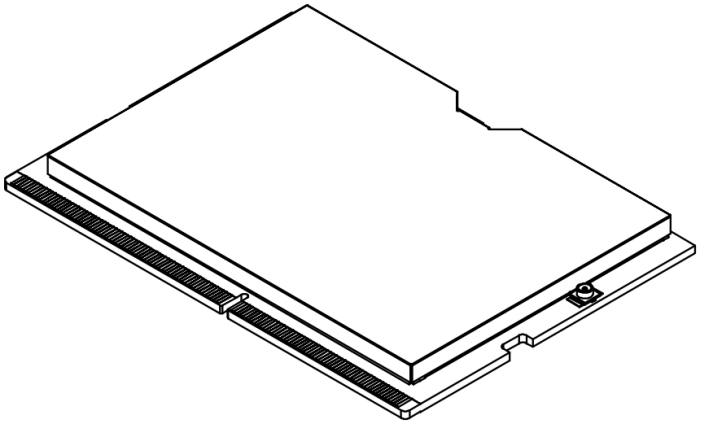
52	VDD_+5V	Power	Input Main Power DC +5V
54	VDD_+5V	Power	Input Main Power DC +5V
56	VDD_+5V	Power	Input Main Power DC +5V
58	VDD_+5V	Power	Input Main Power DC +5V
60	VDD_+5V	Power	Input Main Power DC +5V
62	VDD_+5V	Power	Input Main Power DC +5V
64	VDD_+5V	Power	Input Main Power DC +5V
66	GND	Power	Ground
68	GND	Power	Ground
70	GND	Power	Ground
72	GND	Power	Ground
74	GND	Power	Ground
76	GND	Power	Ground
78	GND	Power	Ground
80	GND	Power	Ground
82	GND	Power	Ground
84	GND	Power	Ground
86	GND	Power	Ground
88	GND	Power	Ground
90	GND	Power	Ground
92	GND	Power	Ground
94	GND	Power	Ground
96	GND	Power	Ground
98	GND	Power	Ground
100	GND	Power	Ground
102	GND	Power	Ground
104	GND	Power	Ground
106	GND	Power	Ground
108	GND	Power	Ground
110	GND	Power	Ground
112	GND	Power	Ground
114	GND	Power	Ground
116	GND	Power	Ground
118	GND	Power	Ground
120	GND	Power	Ground
122	GND	Power	Ground
124	GND	Power	Ground
126	GND	Power	Ground

128	GND	Power	Ground
130	PWR_USB3_VBUS	Analog, Input	This pin is not 5V tolerant and must not connect directly to the 5V VBUS voltage on USB link. This pin must be isolated by an external 30 Kohm ±1% resistor so it could see a lower voltage.
132	GND	Power	Ground
134	GND	Power	Ground
136	PWR_USB_VBUS	Analog, Input	Connect an external 30 Kohm ±1% series resistor to USB 2.0 VBUS
138	GND	Power	Ground
140	USB2_ID	Analog, Input	USB 2.0 OTG ID
142	GND	Power	Ground
144	GND	Power	Ground
146	GND	Power	Ground
148	GND	Power	Ground
150	GND	Power	Ground
152	GND	Power	Ground
154	GND	Power	Ground
156	GND	Power	Ground
158	GND	Power	Ground
160	LCD_DE	CMOS, Input/Output	LCDC (RGB) Interface Data Enable
162	LCD_HSYNC	CMOS, Input/Output	LCDC (RGB) Interface Data Horizontal Synchronization Signal
164	LCD_VSYNC	CMOS, Input/Output	LCDC (RGB) Interface Data Vertical Synchronization Signal
166	LCDD22	CMOS, Input/Output	LCDC (RGB) Interface Data 22
168	LCDD21	CMOS, Input/Output	LCDC (RGB) Interface Data 21
170	LCDD17 / I2S5_BCLK	CMOS, Input/Output	LCDC (RGB) Interface Data 17 / Audio Interface #5 bit clock
172	LCDD18	CMOS, Input/Output	LCDC (RGB) Interface Data 18
174	LCDD16 / I2S5_LRCK	CMOS, Input/Output	LCDC (RGB) Interface Data 16 / Audio Interface #5 WS or LR select
176	GND	Power	Ground
178	RGMIIRXC	CMOS, Input	RGMII Interface RX Clock Input
180	RGMIIRXCTL	CMOS, Input	RGMII Interface RX Control
182	RGMIIRD0	CMOS, Input	RGMII Interface RX Data 0
184	RGMIIRD1	CMOS, Input	RGMII Interface RX Data 1

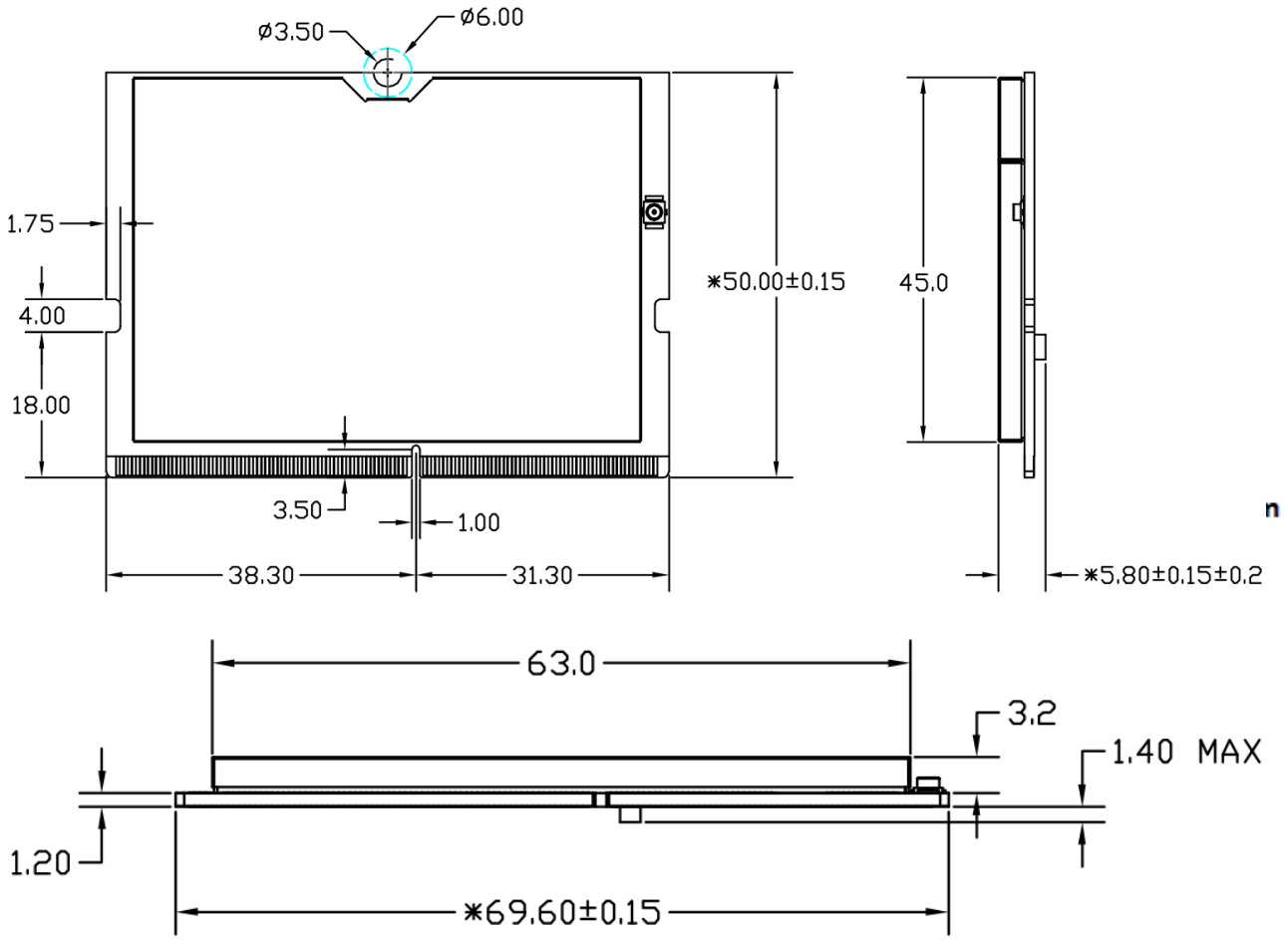
186	RGMIIRD2	CMOS, Input	RGMII Interface RX Data 2
188	RGMIIRD3	CMOS, Input	RGMII Interface RX Data 3
190	GND	Power	Ground
192	RGMIITXC	CMOS, Output	RGMII Interface TX Clock Output
194	RGMIITXCTL	CMOS, Output	RGMII Interface TX Control
196	RGMIITD0	CMOS, Output	RGMII Interface TX Data 0
198	RGMIITD1	CMOS, Output	RGMII Interface TX Data 1
200	RGMIITD2	CMOS, Output	RGMII Interface TX Data 2
202	RGMIITD3	CMOS, Output	RGMII Interface TX Data 3
204	GND	Power	Ground
206	RGMII_CLK_OUT	CMOS, Output	RGMII PHY Clock Reference Output, 25MHz
208	RGMII_MDC	CMOS, Output	RGMII Management Interface Clock
210	RGMII_MDIO	CMOS, Input/Output	RGMII Management Interface Data
212	GND	Power	Ground
214	PWM[3]	CMOS, Output	Pulse-Width Modulation output data 3
216	PWM[2]	CMOS, Output	Pulse-Width Modulation output data 2
218	PWM[0]	CMOS, Output	Pulse-Width Modulation output data 0
220	PWM[1]	CMOS, Output	Pulse-Width Modulation output data 1
222	GND	Power	Ground
224	TW2_SCL	CMOS, Input/Output	TWSI2 Serial clock
226	TW2_SDA	CMOS, Input/Output	TWSI2 Serial data
228	GND	Power	Ground
230	SPI1_SDI	CMOS, Input	SPI1 serial data input / External SPI Bootloader
232	SPI1_SCLK	CMOS, Output	SPI1 serial clock / External SPI Bootloader
234	SPI1_SDO	CMOS, Input/Output	SPI1 serial data output /External SPI Bootloader
236	SPI1_SS1n	CMOS, Output	SPI1 Module select 1 For second slave device with handler.
238	SPI1_SS0n	CMOS, Output	SPI1 Module select 0 / External SPI Bootloader For first slave device with handler
240	GND	Power	Ground
242	JTAG_TDO	CMOS, Output with internal pull-up	JTAG SDATA OUT
244	RSTIn	CMOS, Input with internal pull-up	SoM Active low reset input with internal pullup

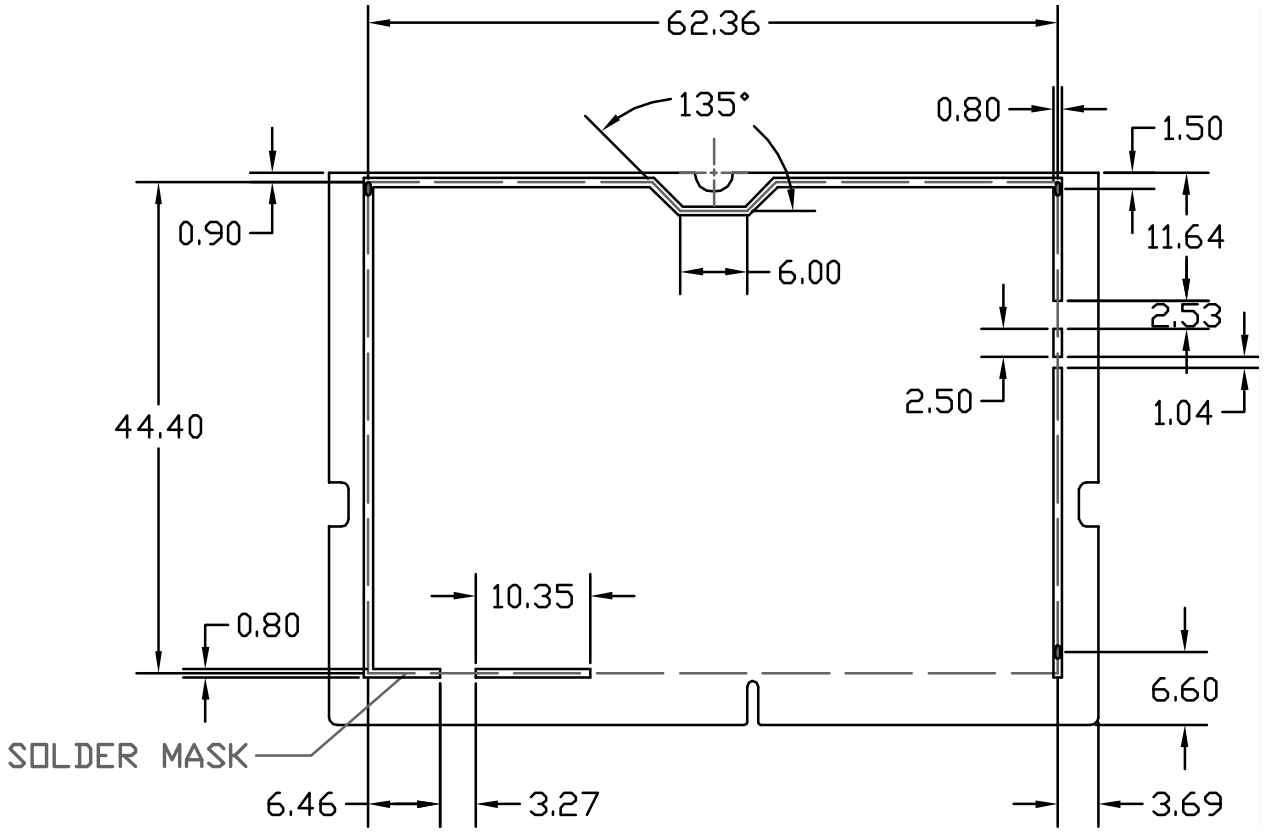
246	JTAG_TDI	CMOS, Input with internal pull-up	JTAG SDATA IN.
248	JTAG_TMS	CMOS, Input with internal pull-up	JTAG Mode select signal
250	JTAG_TCK	CMOS, Input with internal pull-down	JTAG Clock.
252	GND	Power	Ground
254	TW1_SDA	CMOS, Input/Output	TWSI1 Serial data
256	TW1_SCL	CMOS, Input/Output	TWSI1 Serial clock
258	GND	Power	Ground
260	GND	Power	Ground

6.3 Physical Dimensions



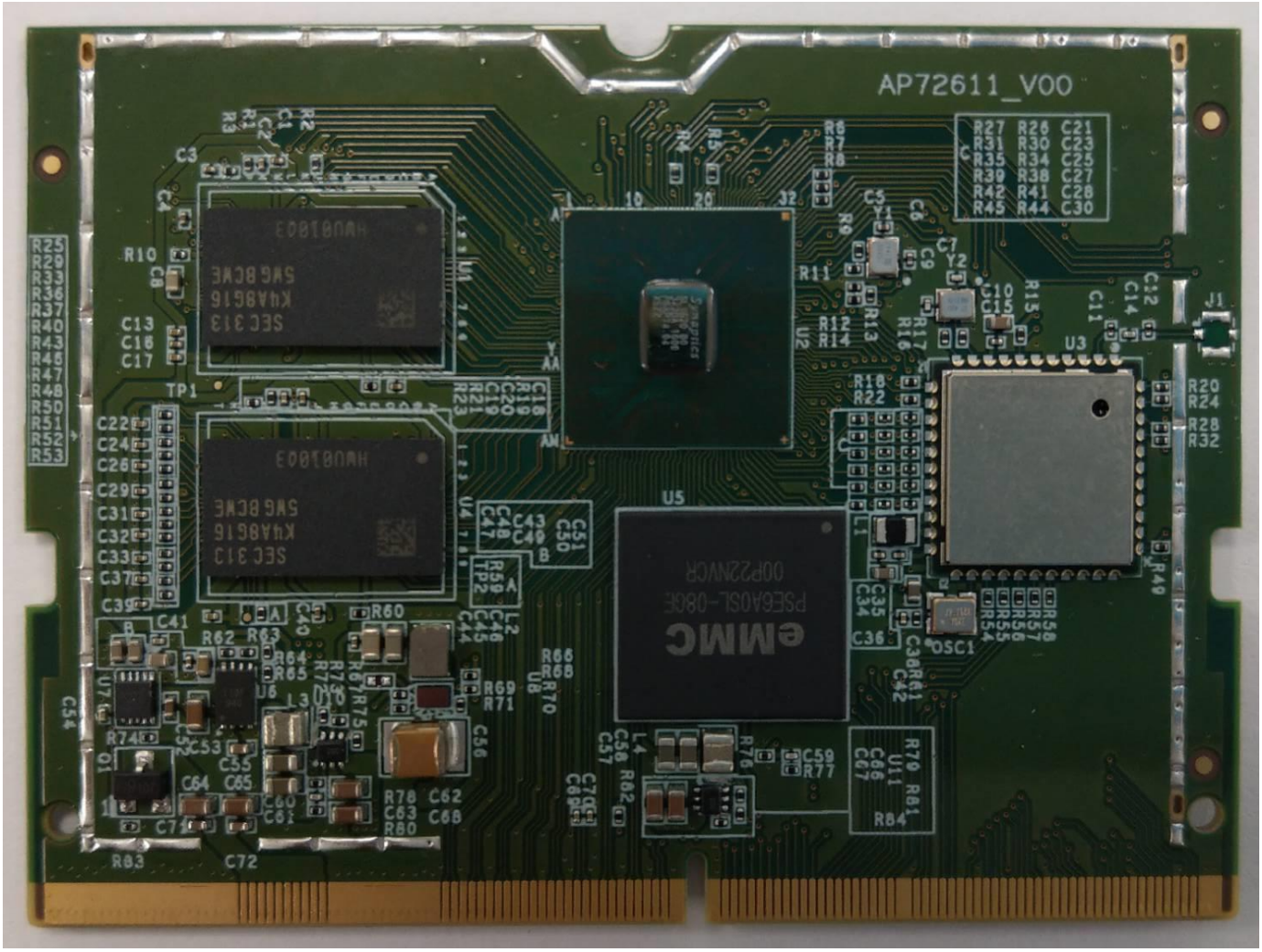
ISOMATRIC VIEW
SCALE 1:1



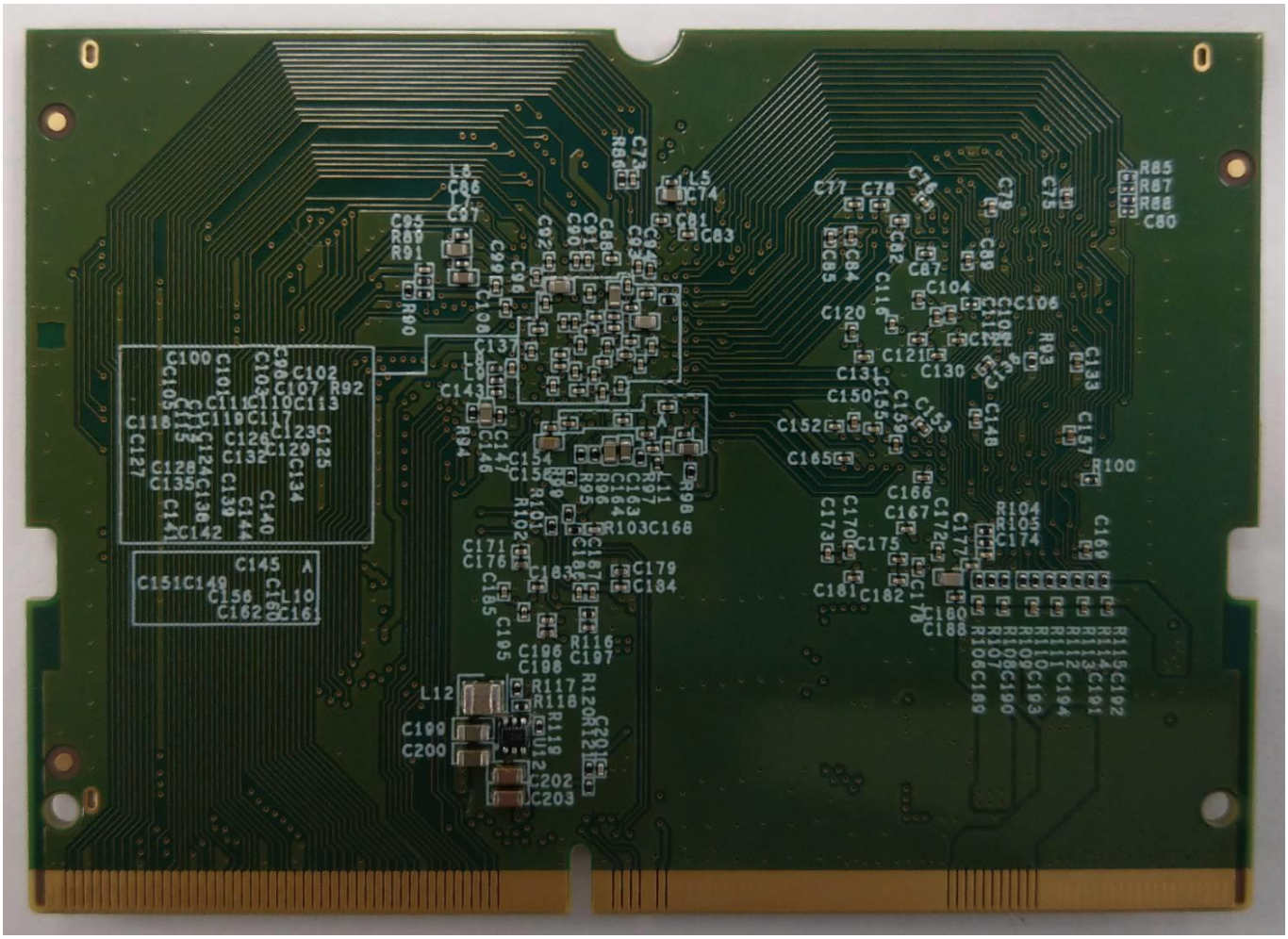

62.36
135°
0.80
1.50
0.90
11.64
6.00
2.53
2.50
1.04
44.40
10.35
0.80
6.60
SOLDER MASK
6.46
3.27
3.69

6.4 Sample Picture

< TOP VIEW >

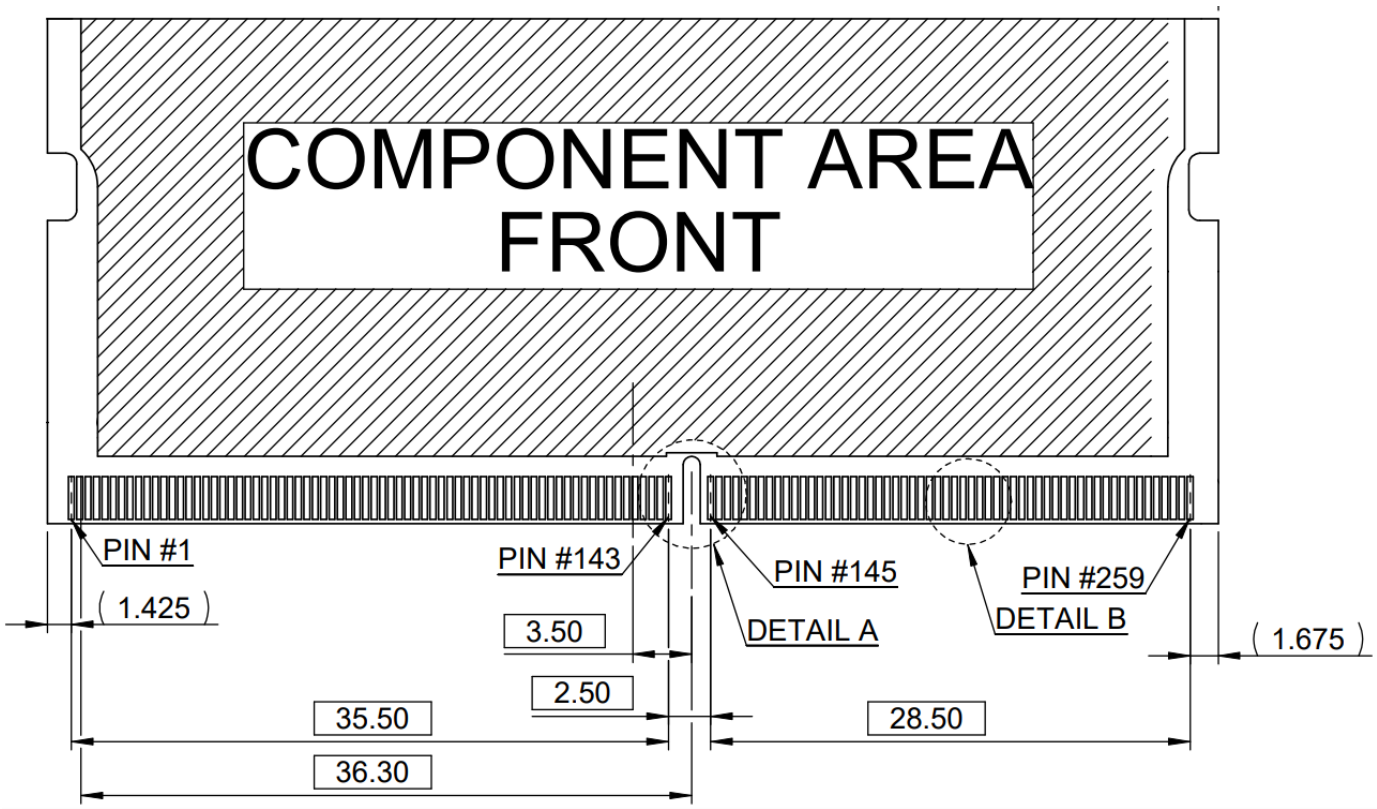


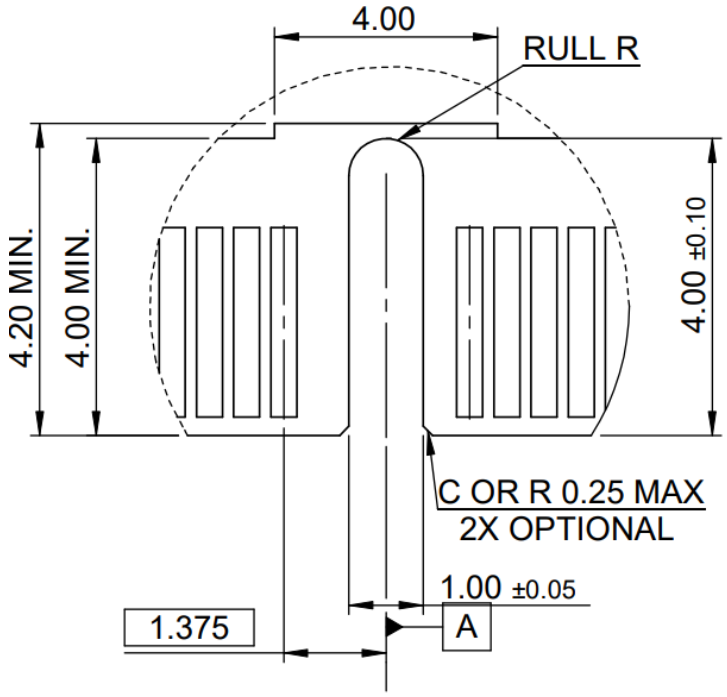
< BOT VIEW >



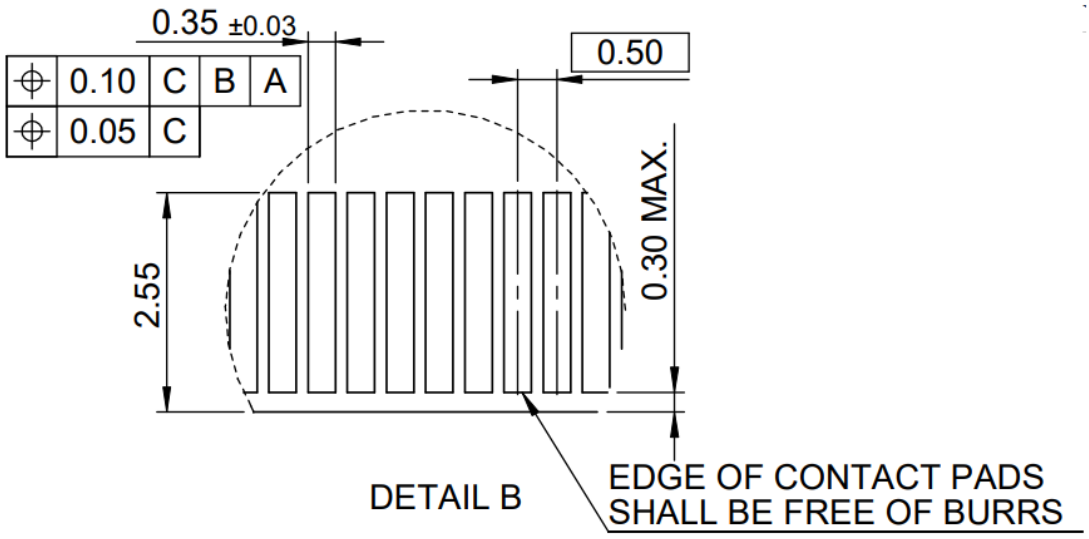
6.5 Pin position

< TOP VIEW >

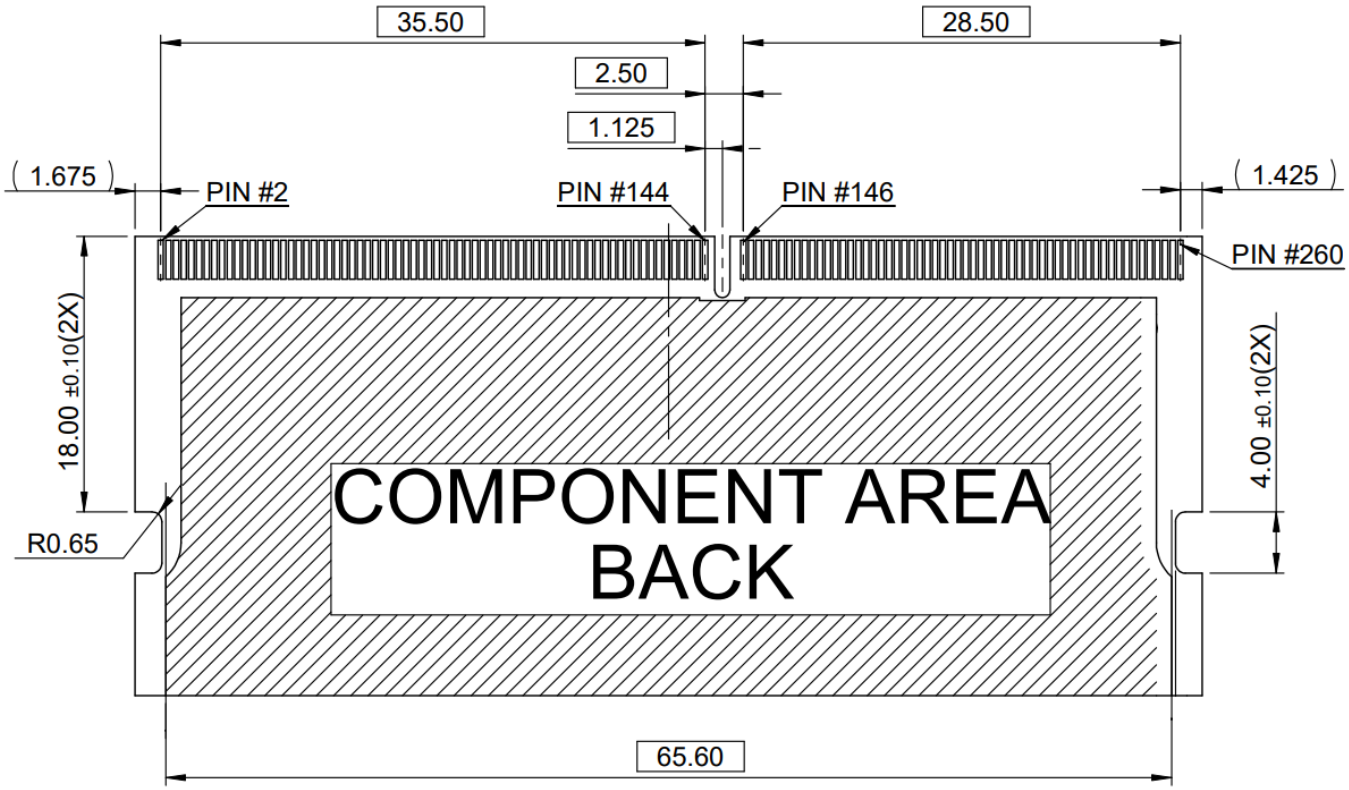




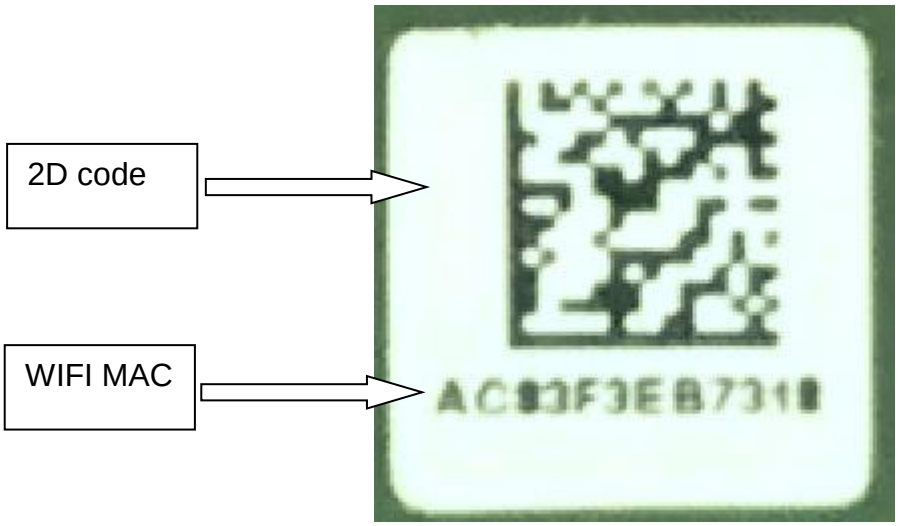
DETAIL A


0.35 ±0.03
0.10 C B A
0.05 C
0.50
0.30 MAX.
2.55
DETAIL B
EDGE OF CONTACT PADS
SHALL BE FREE OF BURRS

< BOT VIEW >


35.50
28.50
2.50
1.125
1.675
PIN #2
PIN #144
PIN #146
1.425
PIN #260
18.00 ±0.10(2X)
4.00 ±0.10(2X)
COMPONENT AREA
BACK
R0.65
65.60

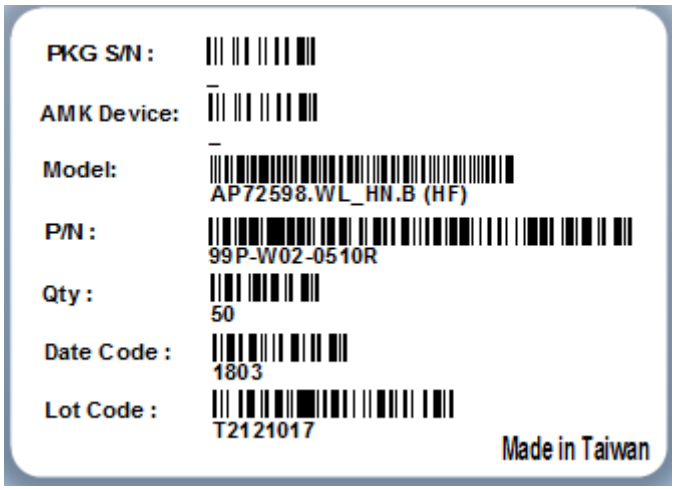
6.6 Label Information



7. Package Information

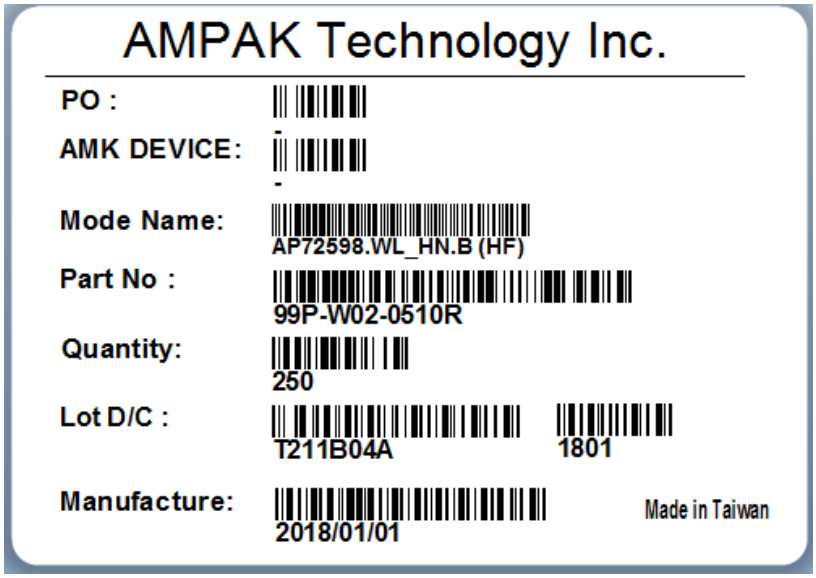
7.1 Label A Inner box label

Label Size: 70mmX50mm
[依各廠實際Label 使用]
(1)Barcode (BC) Symbology: Code128 Auto
(2)Human Readable: Arial
[字高依Label尺寸微調，字體不可斷字,
條碼不可模糊,需可清晰讀取 ,辨識]



7.2 Label B Carton box label

Label Size: 70mm X 100 mm
[依各廠實際Label 使用]
(1)Barcode (BC) Symbology: Code128 Auto
(2)Human Readable: Arial
[字高依Label尺寸微調，字體不可斷字,
條碼不可模糊,需可清晰讀取 ,辨識]



7.3 Package Manner

- 1 防靜電氣泡袋：1 PCS

- 1 BOX：50 PCS

- 1 外箱 CTN：5 BOX　(不滿五箱，使用空箱填滿)

- Label A 黏貼處

Label B 黏貼處

B

8. Carrier Board Information

8.1 Interface

(1) DC to DC Power Input
Connector Type: USB Type-C
Input DC Power Specification: 5V/3A

(2) 4-port USB3.1
Compliant with USB 3.1 Gen 1 Specification Super Speed transmitter/receiver physical layer (PHY) and USB 2.0 High-Speed PHY. It supports Super Speed, Hi-Speed, and Full-Speed USB connections and is fully backward compatible to all USB 2.0 and USB 1.1 hosts.

(3) 1-port USB2.0
Connector Type: USB Type-C
One USB 2.0 On-The-Go (OTG) interface

(4) Video/Display Interfaces
(4-1) RGB:
- Digital Parallel Interface (DPI)
- CPU-type Display Bus Interface (DBI)
- RGB 16bpp (565), 18bpp (666) and 24bpp (888) output formats
- Up to 1080p30 screen resolution and refresh rate

(4-2) MIPI DSI:
- MIPI Display Serial Interface (DSI) with 4-lane DPHY, supports LP and HS modes
- Up to 1080p60 screen resolution and refresh rate

(5) Analog Audio Interface
Right / Left 2-ch Line Output
Full-scale single-ended output : 2.1 VRMS (GND center)

(6) MEMS microphone
2-Channel MEMS microphone with 105dB dynamic range and 69 dB(A) signal-to-noise ratio and Below 1 percent distortions at 128 dBSPL (AOP - 130 dBSPL)
Tight sensitivity (-36 ±1 dB) and phase (± 2 deg) tolerances and 28 Hz low frequency roll-off

(7) USB to Full UART Console Interface
USB Interface: Fully Compliant with USB 2.0 specification (Full-Speed Mode).
UART Interface: Flexible baud rate support up to 12Mbps

(8) Ethernet_RJ-45
1000Base-T IEEE 802.3ab Compliant
100Base-TX IEEE 802.3u Compliant
10Base-T IEEE 802.3 Compliant

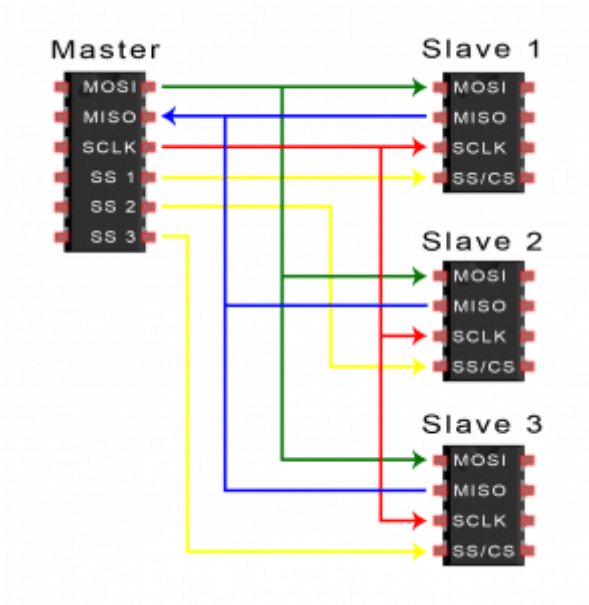
(9) General-purpose input/output
A general-purpose input/output (GPIO) is an uncommitted digital signal pin on an integrated circuit or electronic circuit board which may be used as an input or output, or both, and is controllable by software. GPIOs have no predefined purpose and are unused by default. If used, the purpose and behavior of a GPIO is defined and implemented by the designer of higher assembly-level circuitry: the circuit board designer in the case of integrated circuit GPIOs, or system integrator in the case of board-level GPIOs.

(10) Inter-Integrated Circuit (I2C)
SDA (Serial Data) – The line for the master and slave to send and receive data.
SCL (Serial Clock) – The line that carries the clock signal.
I2C uses only two signals: serial data line (SDA) and serial clock line (SCL). Both are bidirectional and pulled up with resistors. Typical voltages used is +1.8V, although systems with other voltages are permitted.

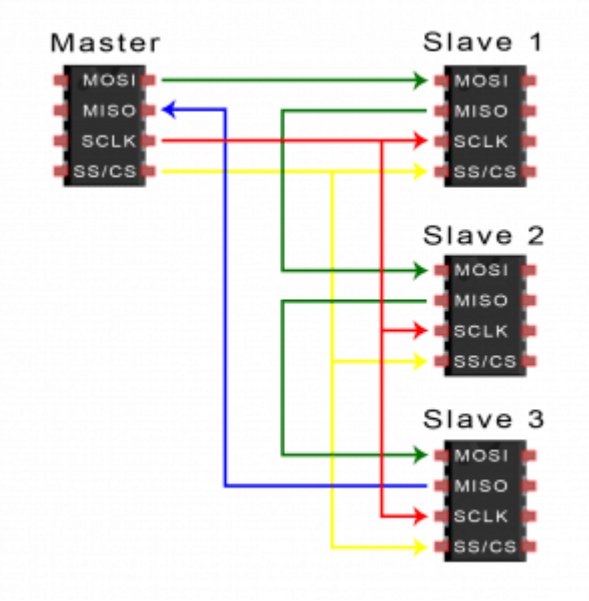
(11) Inter-IC Sound (I2S)
I2S (Inter-IC Sound) is a synchronous, serial communication protocol used for exchanging digital audio data between sound-processing devices.
Support of sample frequencies from 8 to 96/192/384 kHz and slot size 8/16/24/32 bit
Usage of sample frequency 192 kHz limits the TDM interface to 8 channels

(12) Pulse-Width Modulation (PWM)
Pulse width modulation (PWM) is a technique used to precisely control analog devices with a digital signal. A pulse width modulation signal consists of electronic pulses that are used to mimic a changing analog voltage.
PWM Duty Cycle Resolution: min.— 2 ; max.— 16 bit

(13) Serial Peripheral Interface (SPI)
MOSI (Master Output/Slave Input) – Line for the master to send data to the slave.
MISO (Master Input/Slave Output) – Line for the slave to send data to the master.
SCLK (Clock) – Line for the clock signal.
SS/CS (Slave Select/Chip Select) – Line for the master to select which slave to send data to.
Up to four slave devices supported on each interface.
SPI can be set up to operate with a single master and a single slave, and it can be set up with multiple slaves controlled by a single master. There are two ways to connect multiple slaves to the master. If the master has multiple slave select pins, the slaves can be wired in parallel like this:

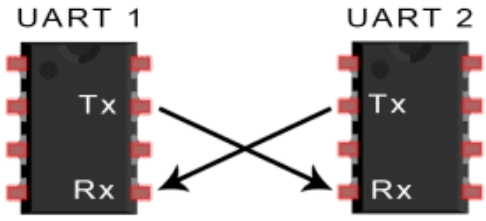


If only one slave select pin is available, the slaves can be daisy-chained like this:



(15) Universal Asynchronous Receiver/Transmitter (UART)

In UART communication, two UARTs communicate directly with each other. The transmitting UART converts parallel data from a controlling device like a CPU into serial form, transmits it in serial to the receiving UART, which then converts the serial data back into parallel data for the receiving device. Only two wires are needed to transmit data between two UARTs. Data flows from the Tx pin of the transmitting UART to the Rx pin of the receiving UART:



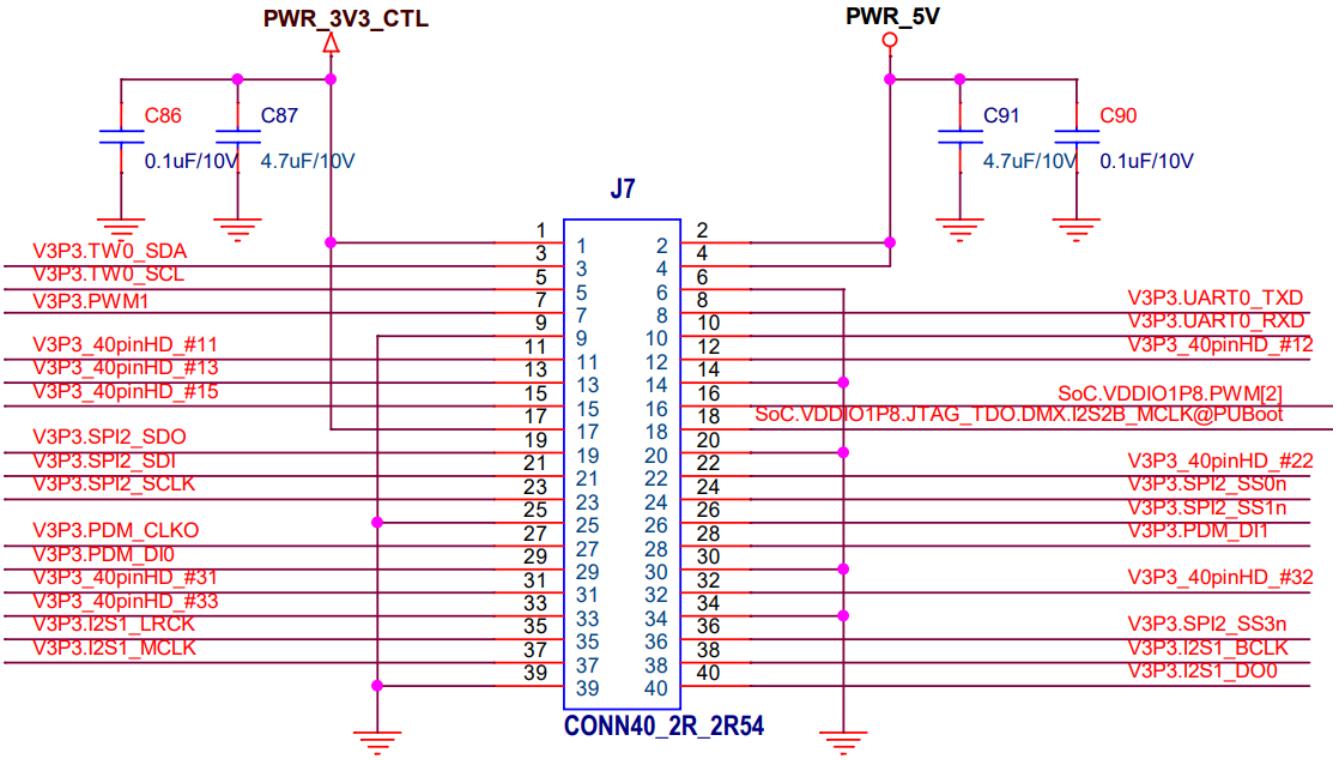
(16) Pulse Density Modulation (PDM)

PDM is used to convert an analog signal voltage into a single-bit pulse density modulated digital stream. PDM signals look more akin to a longitudinal wave than the stereotypical transverse wave that is associated with audio, but they are a digital representation of an analog signal.

8.2 Expansion interface

(1) Connector Type: pitch 2.54mm pin header dual row straight

(2) Pin define:

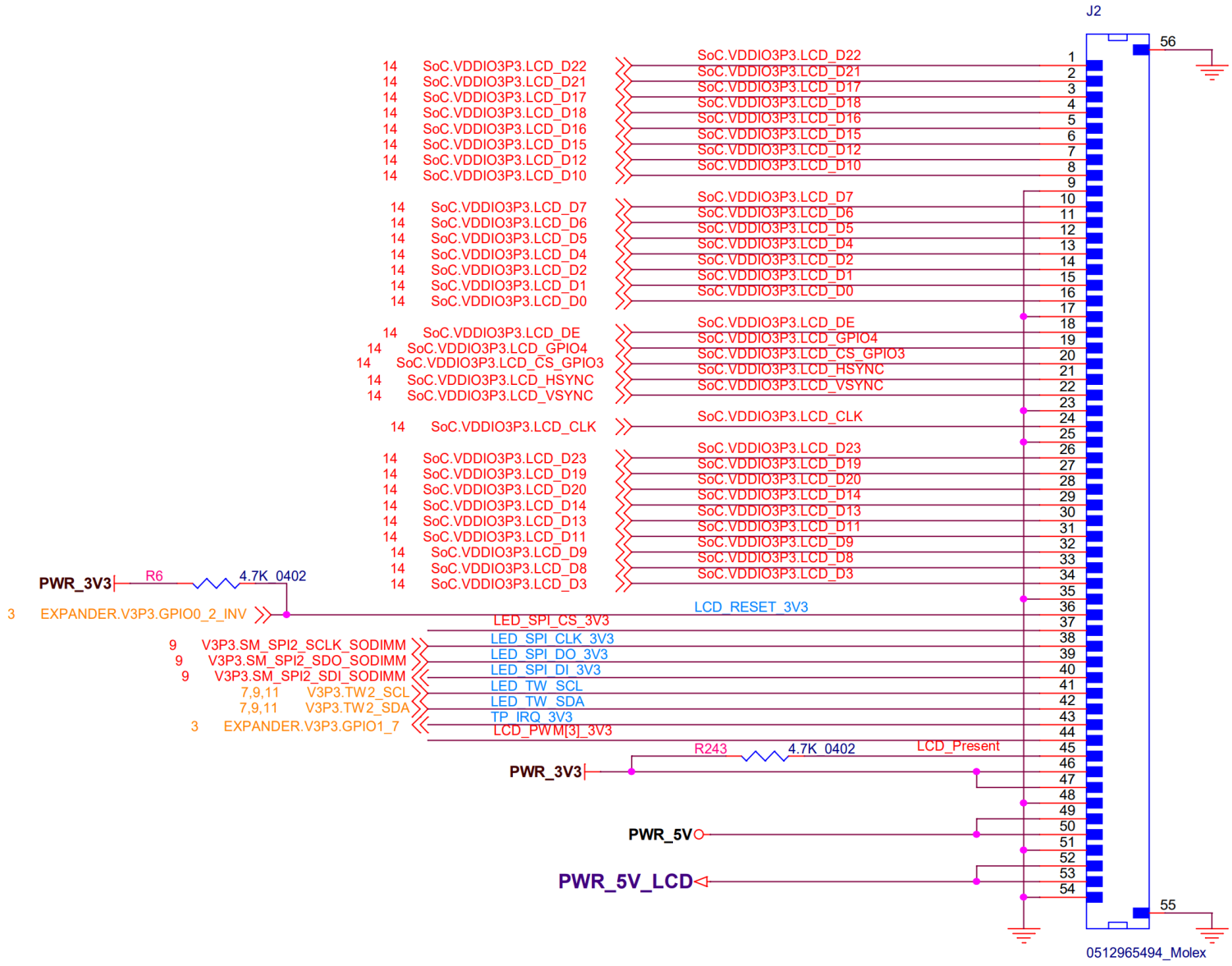


Expansion interface_40 pin header (Odd number)			
Pin #	**Pin Name**	**Pin Type**	**Description**
1	PWR_3V3_CTL	Power Out	DC Power Supply: 3.3V
3	V3P3.TW0_SDA	I/O	I2C_SDA (Serial Data)
5	V3P3.TW0_SCL	I/O	I2C_SCL (Serial Clock)
7	V3P3.PWM1	I/O	Pulse-Width Modulation-1
9	GND	Ground	
11	V3P3_40pinHD_#11	I/O	V1P8.SoC.TW1.SCL(I2C)
13	V3P3_40pinHD_#13	I/O	V1P8.SoC.TW1.SDA(I2C)
15	V3P3_40pinHD_#15	I/O	SoC.VDDIO1P8.I2S1_DI
17	PWR_3V3_CTL	Power Out	DC Power Supply: 3.3V

19	V3P3.SPI2_SDO	I/O	MOSI (Master Output/Slave Input)
21	V3P3.SPI2_SDI	I/O	MISO (Master Input/Slave Output)
23	V3P3.SPI2_SCLK	I/O	SCLK (Clock)
25	GND	Ground	
27	V3P3.PDM_CLKO	I/O	PDM Clock
29	V3P3.PDM_DI0	I/O	PDM Data-0
31	V3P3_40pinHD_#31	I/O	GPIO Reserved
33	V3P3_40pinHD_#33	I/O	GPIO Reserved
35	V3P3.I2S1_LRCK	I/O	I2S_Left-Right Clock
37	V3P3.I2S1_MCLK	I/O	I2S_Master Clock
39	GND	Ground	

Expansion interface_40 pin header (Even number)			
Pin #	**Pin Name**	**Pin Type**	**Description**
2	PWR_5V	Power Out	DC Power Supply: 5V
4	PWR_5V	Power Out	DC Power Supply: 5V
6	GND	Ground	
8	V3P3.UART0_TXD	I/O	UART_Transmitting Serial Data
10	V3P3.UART0_RXD	I/O	UART_Receiving Serial Data
12	V3P3_40pinHD_#12	I/O	GPIO Reserved
14	GND	Ground	
16	SoC.VDDIO1P8.PWM[2]	I/O	Pulse-Width Modulation-2
18	SoC.VDDIO1P8.JTAG_TDO. DMX.I2S2B_MCLK@PUBoot	I/O	GPIO_Normal
20	GND	Ground	
22	V3P3_40pinHD_#22	I/O	GPIO Reserved
24	V3P3.SPI2_SS0n	I/O	SS/CS (Slave Select/Chip Select)
26	V3P3.SPI2_SS1n	I/O	SS/CS (Slave Select/Chip Select)
28	V3P3.PDM_DI1	I/O	PDM Data-1
30	GND	Ground	
32	V3P3_40pinHD_#32	I/O	GPIO Reserved
34	GND	Ground	
36	V3P3.SPI2_SS3n	I/O	SS/CS (Slave Select/Chip Select)
38	V3P3.I2S1_BCLK	I/O	I2S_Bit Clock Line
40	V3P3.I2S1_DO0	I/O	I2S_Serial Data

8.3 Video Display LCD R/G/B Interface



0.50mm Pitch Easy-On FFC/FPC Connector, 1.30mm Height, Right-Angle, Surface Mount, ZIF, Bottom Contact Style, 54 Circuits, Gold (Au) Contact Plating

Part number :0512965494

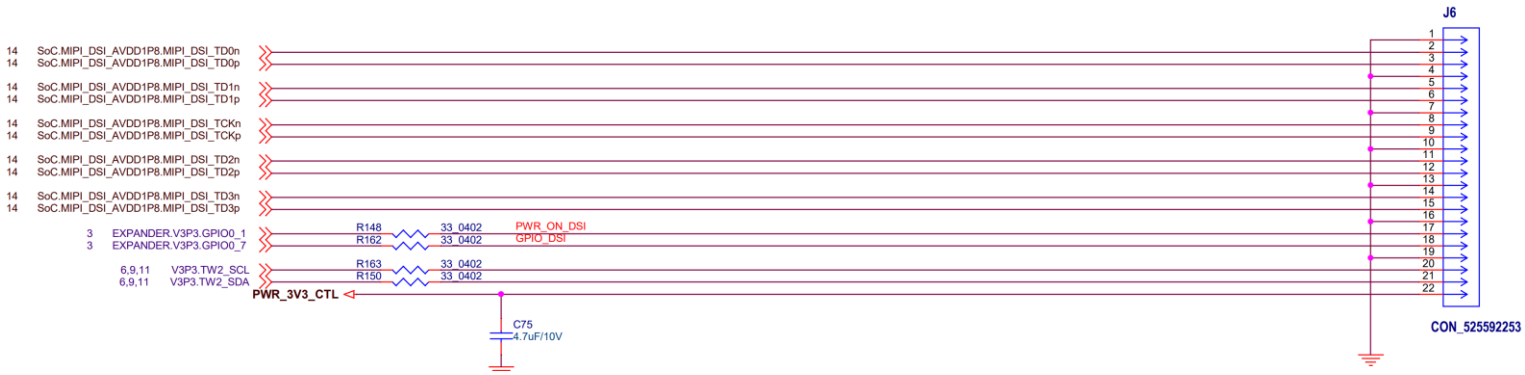
URL:

https://www.molex.com/en-us/products/part-detail/0512965494

Video Display_Liquid Crystal Displays (LCD) R/G/B Interface			
Pin #	**Pin Name**	**Pin Type**	**Description**
1	SoC.VDDIO3P3.LCD_D22	I/O	LCD panel Data Bus_D22
2	SoC.VDDIO3P3.LCD_D21	I/O	LCD panel Data Bus_D21
3	SoC.VDDIO3P3.LCD_D17	I/O	LCD panel Data Bus_D17
4	SoC.VDDIO3P3.LCD_D18	I/O	LCD panel Data Bus_D18
5	SoC.VDDIO3P3.LCD_D16	I/O	LCD panel Data Bus_D16
6	SoC.VDDIO3P3.LCD_D15	I/O	LCD panel Data Bus_D15
7	SoC.VDDIO3P3.LCD_D12	I/O	LCD panel Data Bus_D12
8	SoC.VDDIO3P3.LCD_D10	I/O	LCD panel Data Bus_D10
9	GND	Ground	Power Ground
10	SoC.VDDIO3P3.LCD_D7	I/O	LCD panel Data Bus_D7
11	SoC.VDDIO3P3.LCD_D6	I/O	LCD panel Data Bus_D6
12	SoC.VDDIO3P3.LCD_D5	I/O	LCD panel Data Bus_D5
13	SoC.VDDIO3P3.LCD_D4	I/O	LCD panel Data Bus_D4
14	SoC.VDDIO3P3.LCD_D2	I/O	LCD panel Data Bus_D2
15	SoC.VDDIO3P3.LCD_D1	I/O	LCD panel Data Bus_D1
16	SoC.VDDIO3P3.LCD_D0	I/O	LCD panel Data Bus_D0
17	GND	Ground	Power Ground
18	SoC.VDDIO3P3.LCD_DE	I	LCD panel Data Enable
19	SoC.VDDIO3P3.LCD_GPIO4	I/O	LCD panel Normal GPIO4
20	SoC.VDDIO3P3.LCD_CS_GPIO3	I/O	LCD panel Normal GPIO3
21	SoC.VDDIO3P3.LCD_HSYNC	I/O	LCD panel Horizontal Synchronization
22	SoC.VDDIO3P3.LCD_VSYNC	I/O	LCD panel Vertical Synchronization
23	GND	Ground	Power Ground
24	SoC.VDDIO3P3.LCD_CLK	I/O	LCD panel Clock
25	GND	Ground	Power Ground
26	SoC.VDDIO3P3.LCD_D23	I/O	LCD panel Data Bus_D23
27	SoC.VDDIO3P3.LCD_D19	I/O	LCD panel Data Bus_D19
28	SoC.VDDIO3P3.LCD_D20	I/O	LCD panel Data Bus_D20
29	SoC.VDDIO3P3.LCD_D14	I/O	LCD panel Data Bus_D14
30	SoC.VDDIO3P3.LCD_D13	I/O	LCD panel Data Bus_D13
31	SoC.VDDIO3P3.LCD_D11	I/O	LCD panel Data Bus_D11
32	SoC.VDDIO3P3.LCD_D9	I/O	LCD panel Data Bus_D9
33	SoC.VDDIO3P3.LCD_D8	I/O	LCD panel Data Bus_D8
34	SoC.VDDIO3P3.LCD_D3	I/O	LCD panel Data Bus_D3

35	GND	Ground	Power Ground
36	LCD_RESET_3V3	I/O	LCD panel Global reset pin
37	LED_SPI_CS_3V3	I/O	LCD panel SPI interface Chip Select
38	LED_SPI_CLK_3V3	I/O	LCD panel SPI interface Clock
39	LED_SPI_DO_3V3	I/O	LCD panel SPI interface Data Output
40	LED_SPI_DI_3V3	I/O	LCD panel SPI interface Data Input
41	LED_TW_SCL	I/O	LCD panel I2C interface Clock
42	LED_TW_SDA	I/O	LCD panel I2C interface Data
43	TP_IRQ_3V3	I/O	Interrupt signal for TP
44	LCD_PWM[3]_3V3	I/O	LCD panel Pulse-Width Modulation
45	LCD_Present	I/O	LCD panel Presentation Screens Control pin
46	PWR_3V3	Power	Power for Digital Circuit : DC 3.3V
47	PWR_3V3	Power	Power for Digital Circuit : DC 3.3V
48	GND	Ground	Power Ground
49	PWR_5V	Power	Power for Digital Circuit : DC 5.0V
50	PWR_5V	Power	Power for Digital Circuit : DC 5.0V
51	GND	Ground	Power Ground
52	PWR_5V_LCD	Power	Power for Backlight Circuit : DC 5.0V
53	PWR_5V_LCD	Power	Power for Backlight Circuit : DC 5.0V
54	GND	Ground	Power Ground
55	GND	Ground	Power Ground
56	GND	Ground	Power Ground

8.4 Video Display MIPI Interface



Easy-On FFC/FPC Connector, 0.50mm Pitch, Slider Series, Vertical, 3.90mm Height, 22 Circuits, Gold Plating

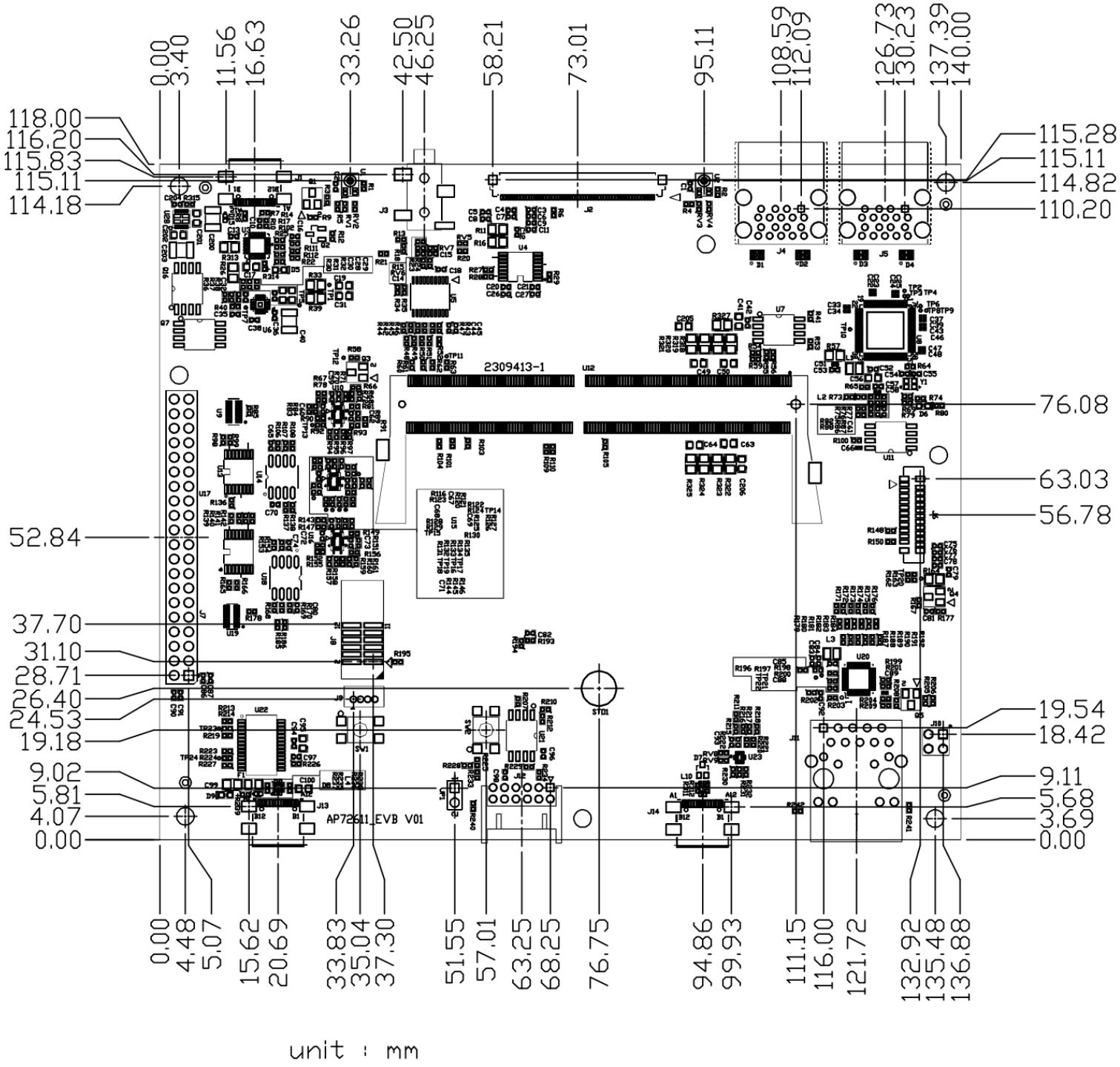
Part Number: 525592253

URL:

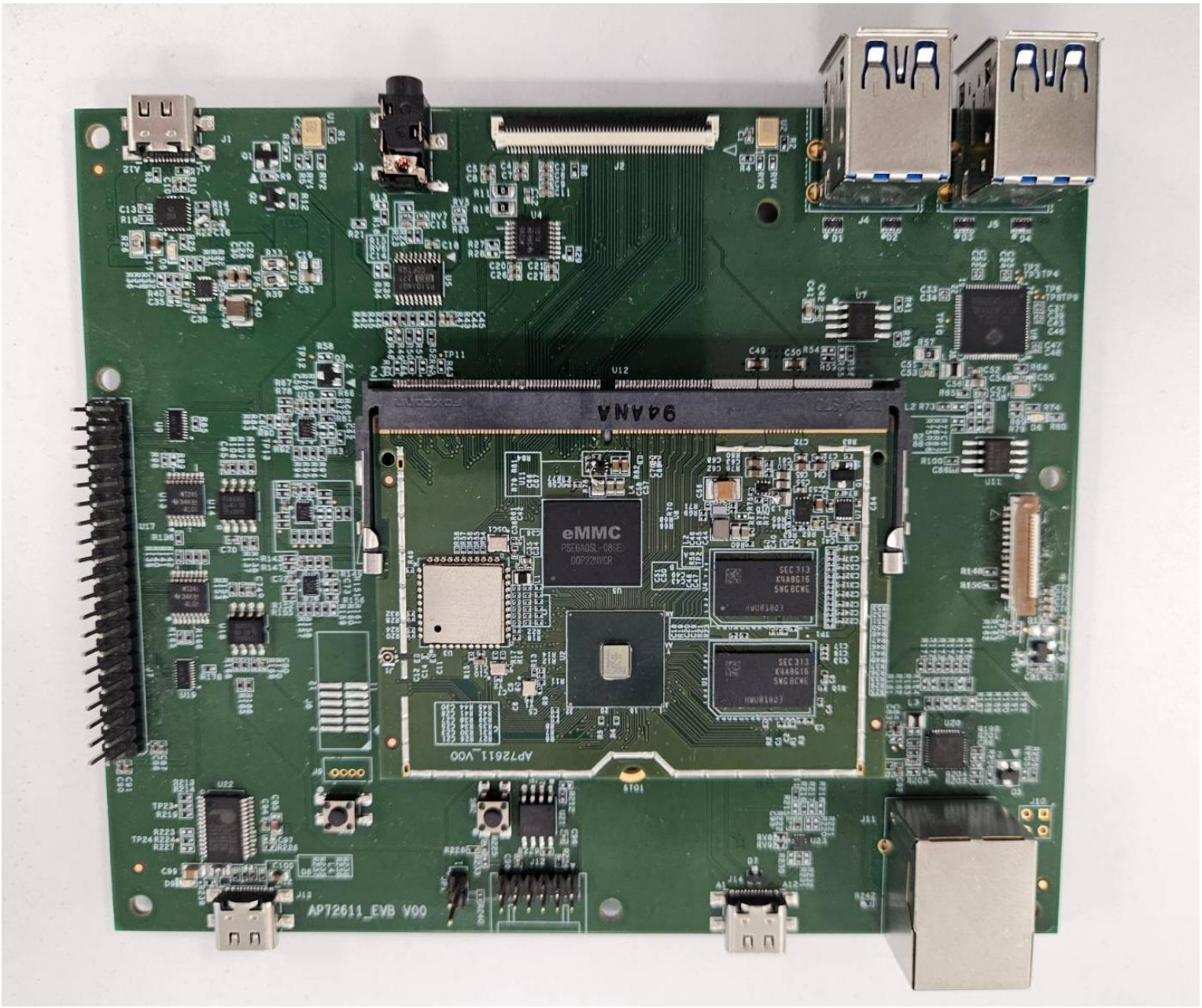
https://www.molex.com/en-us/products/part-detail/525592253

Video Display_Mobile Industry Processor Interface (MIPI) Interface			
Pin #	**Pin Name**	**Pin Type**	**Description**
1	GND	Ground	Power Ground
2	SoC.MIPI_DSI_AVDD1P8.MIPI_DSI_TD0n	O	Negative MIPI differential data0 input
3	SoC.MIPI_DSI_AVDD1P8.MIPI_DSI_TD0p	O	Positive MIPI differential data0 input
4	GND	Ground	Power Ground
5	SoC.MIPI_DSI_AVDD1P8.MIPI_DSI_TD1n	O	Negative MIPI differential data1 input
6	SoC.MIPI_DSI_AVDD1P8.MIPI_DSI_TD1p	O	Positive MIPI differential data1 input
7	GND	Ground	Power Ground
8	SoC.MIPI_DSI_AVDD1P8.MIPI_DSI_TCKn	O	Negative MIPI differential clock input
9	SoC.MIPI_DSI_AVDD1P8.MIPI_DSI_TCKp	O	Positive MIPI differential clock input
10	GND	Ground	Power Ground
11	SoC.MIPI_DSI_AVDD1P8.MIPI_DSI_TD2n	O	Negative MIPI differential data2 input
12	SoC.MIPI_DSI_AVDD1P8.MIPI_DSI_TD2p	O	Positive MIPI differential data2 input
13	GND	Ground	Power Ground
14	SoC.MIPI_DSI_AVDD1P8.MIPI_DSI_TD3n	O	Negative MIPI differential data3 input
15	SoC.MIPI_DSI_AVDD1P8.MIPI_DSI_TD3p	O	Positive MIPI differential data3 input
16	GND	Ground	Power Ground
17	EXPANDER.V3P3.GPIO0_1	I/O	Reserved GPIO pin
18	EXPANDER.V3P3.GPIO0_7	I/O	Reserved GPIO pin
19	GND	Ground	Power Ground
20	V3P3.TW2_SCL	O	I2C Serial clock output
21	V3P3.TW2_SDA	I/O	I2C Serial data input/output
22	PWR_3V3_CTL	Power	Power supply output 3.3V

8.5 Board Dimension



8.6 Board Pictures



9. Note